REMARKS

Claims 1-3, 5-9, 11-15, and 17-18 are pending in this application. Claims 1-3, 5-9, 11-15, and 17-18 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,651,106 to Ashburn (hereinafter "Ashburn"). Applicants thank the Examiner for the telephonic interview conducted with the undersigned on October 2, 2003. During the interview, the present invention was explained in connection with Figure 6. A proposed amended claim 1 was discussed, but no decision was made during the interview on whether such amendments would distinguish the present invention over the cited art. The Examiner had indicated that the claims needed to be more specific.

By the foregoing amendments, Applicants have amended the claims to further define and clarify the operation of the present invention. Applicants note that claim 1 as amended herein differs from the proposed amended claim 1 discussed with the Examiner during the interview. The independent claims (i.e., claims 1, 7, and 13) have been amended to clarify that each task to be performed on the image data includes one or more basic state operations, each basic state operation being a single arithmetic operation, and that the state operations are filtered according to arithmetic operation type prior to the state operations being performed. Dependent claims 4, 10, and 16 have been canceled, as the subject

matter contained in those claims has been incorporated into independent claims 1, 7, and 13, respectively.

Ashburn discloses a method and apparatus for generating triangles that can be easily filled by a triangle fill scan converter. The apparatus includes a front end board 10 for receiving graphics primitives to be rendered, with each primitive being specified by coordinate data, color data, and texture data. A frame buffer board 14 interpolates the primitive data to generate the image to be displayed on a screen. Both the front end board 10 and the frame buffer board 14 are pipelined to be able to operate on multiple primitives simultaneously (see column 4, lines 36-66). In one embodiment of Ashburn, certain hardware components may be duplicated to increase the bandwidth of the system (see column 7, lines 56-60).

The present invention relates to a method and apparatus for processing video image data, including position data, color data, and texture data. Different tasks (e.g., moving or scaling) can be performed on each image data type. Each task consists of a series of basic state operations that may need to be performed in a particular sequence. Each basic state operation is a single arithmetic operation, such as addition or multiplication. To quickly process image data, the present invention provides a common arithmetic unit for each basic state operation type. The basic state operations are filtered based upon the arithmetic operation type, regardless of what task the operation originated from. These basic state operations

are then queued for the appropriate common arithmetic unit and performed. Unless a task requires that the basic state operations be performed in a particular order, basic state operations relating to different tasks can be concurrently performed by different arithmetic units. (See page 6, lines 1-12.)

The present invention differs from Ashburn in that Ashburn does not filter the image data by the basic state operation to be performed on the data. In regard to the rejection of claim 1, the portions of Ashburn cited by the Examiner do not disclose the present invention. Figure 12 "shows several examples of triangles having different sort results" (see column 18, lines 16-17). The triangles are sorted according to Y-axis values to assist in processing them (see column 13, lines 5-10 and 16-20). However, the data that defines the triangles is not broken down according to the basic state operation to be performed on the data, as is done in the present invention.

In Figure 16, Ashburn discloses a memory map for a register file 180 used to store the data pertaining to each vertex of a triangle; there is no mention of filtering the data other than as a triangle vertex (see Figure 16 and column 19, lines 52-66).

> According to one aspect of the invention, the graphics system divides a quadrilateral into two triangles so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. (Column 9, lines 56-60, emphasis added.)

Based on this statement, the Ashburn apparatus only performs arithmetic operations on data in a particular sequence. If all the equations for the first triangle have not been completed, it would not be possible to achieve the efficiencies desired by this apparatus. Contrast this with the present invention, in which the basic state operations do not always have to be performed in a particular order, and multiple different basic state operations relating to the same image data group can be simultaneously performed.

The same remarks as applied to claim 1 are equally applicable to the Examiner's rejections of independent claims 7 and 13. Because the independent claims (i.e., claims 1, 7, and 13) of the present invention are distinguishable over Ashburn, the dependent claims (i.e., claims 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, and 18) should also be distinguishable over Ashburn and no further discussion of the dependent claims is needed.

In regard to the Examiner's response to Applicants' arguments filed on May 9, 2003, Applicants note that the basic state operation equations for the position data, color data, and texture data are shown in the tables in Figures 3a, 4a, and 5a, respectively. In regard to the Examiner's interpretation that "texture data comprises color data," Applicants note that texture information can include information "such as the pixel's texture pattern and the depth of the pattern from the viewer" (page 1, lines 8-9).

In regard to the Examiner's discussion of the equations disclosed in Ashburn (column 10, line 9 through column 11, line 43), Applicants note that these equations consist of multiple operations per equation. This is direct contrast to the present application, in which the basic state operations each consist of a single arithmetic operation, as shown in Figures 3a, 4a, and 5a.

In regard to the Examiner's discussion of the geometry accelerator chips 32A, 32B, and 32C, while the functionality of these chips may permit the calculations to be completed faster, the calculations for the first triangle still must be completed prior to proceeding with the calculations for other triangles.

> Each 3-D geometry accelerator chip transforms the x, y, z coordinates that define the primitives received into corresponding screen space coordinates, determines object R, G, B values and texture S, T values for the screen space coordinates, decomposes primitive quadrilaterals into triangles, computes a triangle plane equation to define each triangle, and computes light source calculations to determine R, G, B values.

Column 5, lines 20-27. The triangle plane equations are discussed from column 13, line 11 to column 15, line 22. Most of the triangle plane equations described in Ashburn contain more than one arithmetic operation, as opposed to the present invention, in which the basic state operations each consist of a single arithmetic operation. Even with the accelerator chips, Ashburn still calls for more complicated operations than the present invention and still requires that the

operations for a first triangle be completed before starting the operations for subsequent triangles.

It is respectfully submitted that the amendments and remarks made herein place pending claims 1-3, 5-9, 11-15, and 17-18 in condition for allowance. Accordingly, entry of this amendment as well as reconsideration and allowance of pending claims 1-3, 5-9, 11-15, and 17-18 are respectfully requested.

If the Examiner does not believe that the claims are in condition for allowance, the Examiner is respectfully requested to contact the undersigned at 215-568-6400.

Respectfully submitted,

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